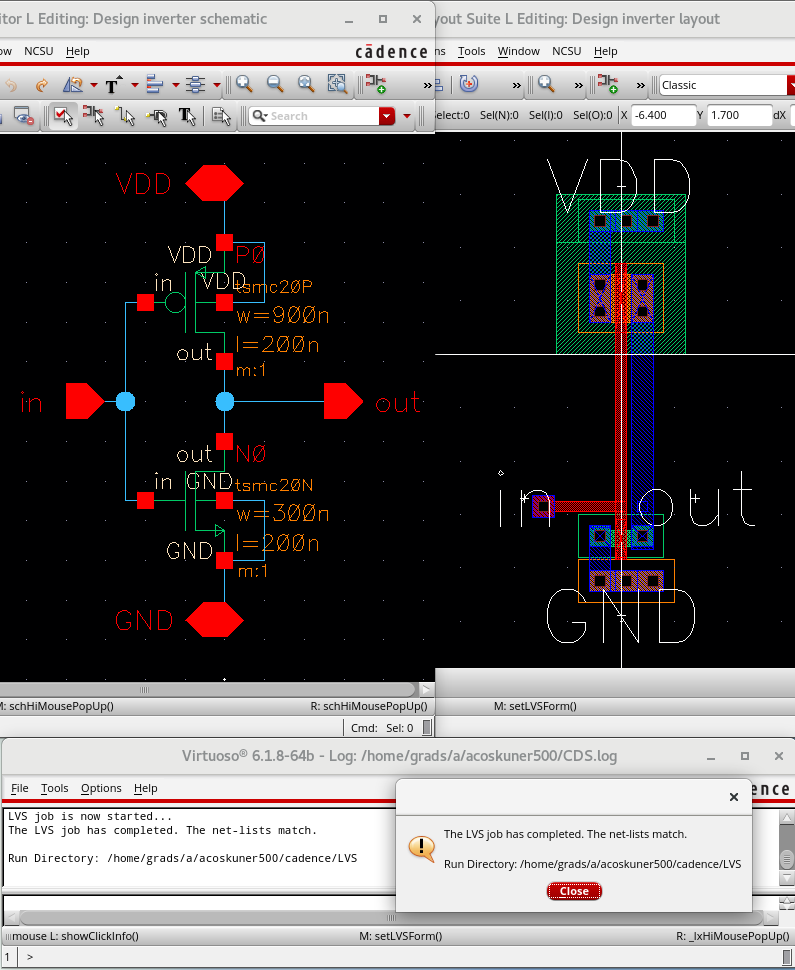
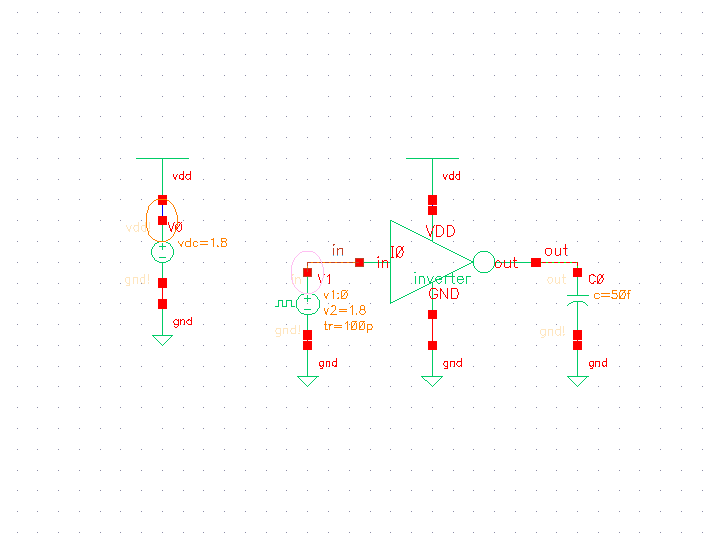
**ECEN 714-612 Lab 4**

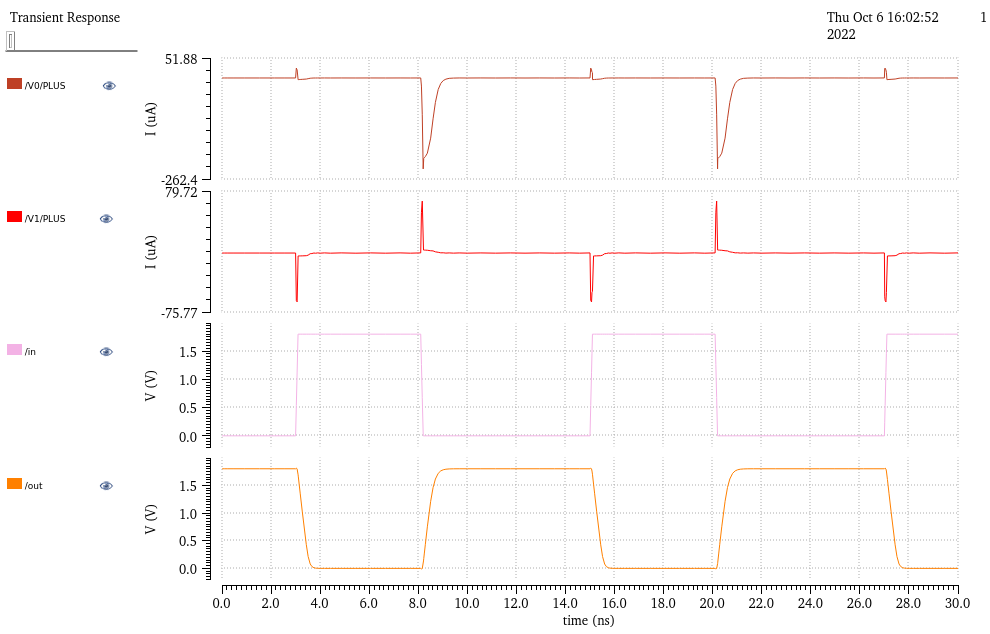
1. Inverter Changes (Schematic, Layout, LVS)



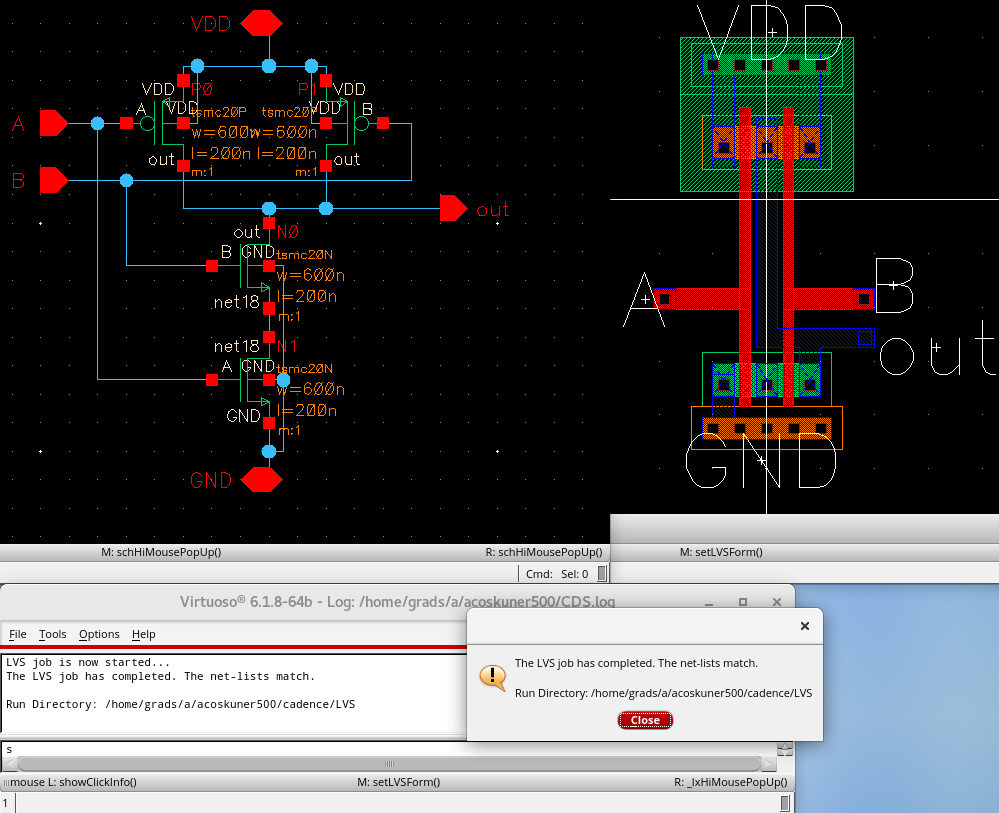
1. Inverter simulation

| Inverter power VDD | -11.60E-6 |
| --- | --- |
| Inverter vpulse average power | -183.2E-9 |
| Inverter rising delay | 8.150E-9 264.1E-12  20.15E-9 264.1E-12 |
| Inverter falling delay | 3.050E-9 257.1E-12  15.05E-9 257.1E-12  27.05E-9 257.1E-12 |



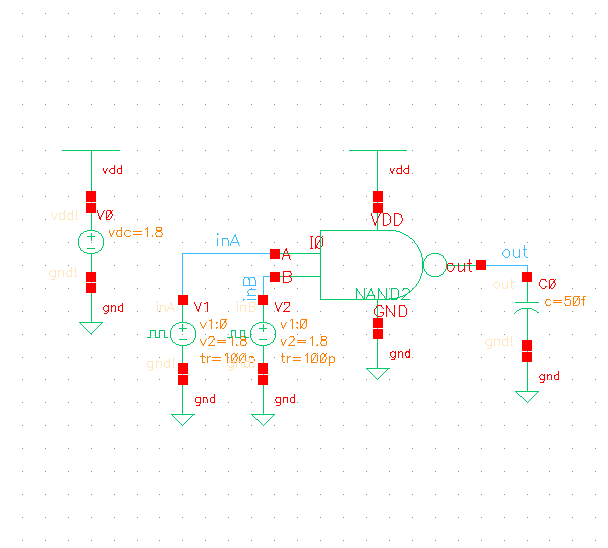


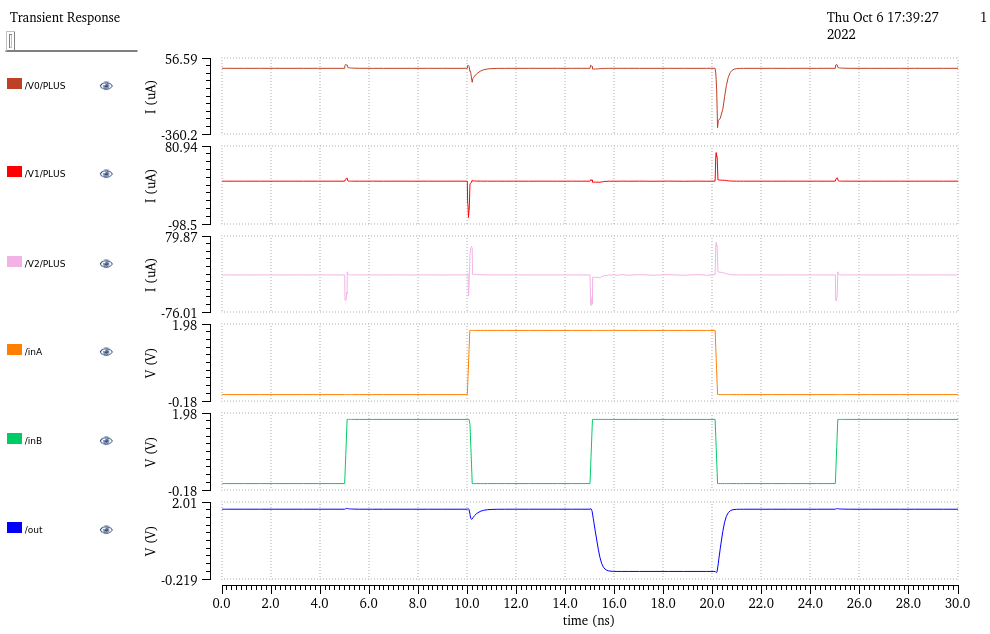
1. NAND2 Changes (Schematic, Layout, LVS)



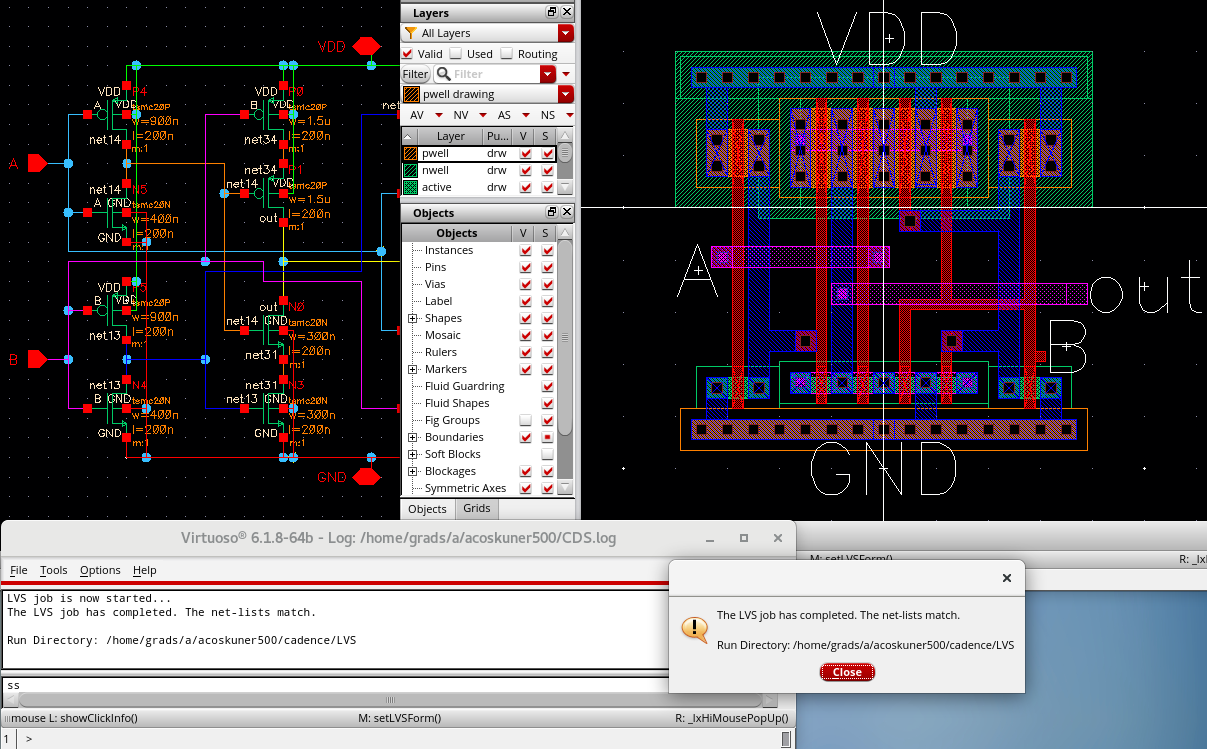
1. NAND2 Simulation

| NAND2 power VDD | -6.865E-6 |
| --- | --- |
| NAND2 inA vpulse average power | 11.46E-9 |
| NAND2 inB vpulse average power | -125.5E-9 |
| NAND2 rising delay | 2.09E-10 |
| NAND2 falling delay | 2.27E-10 |



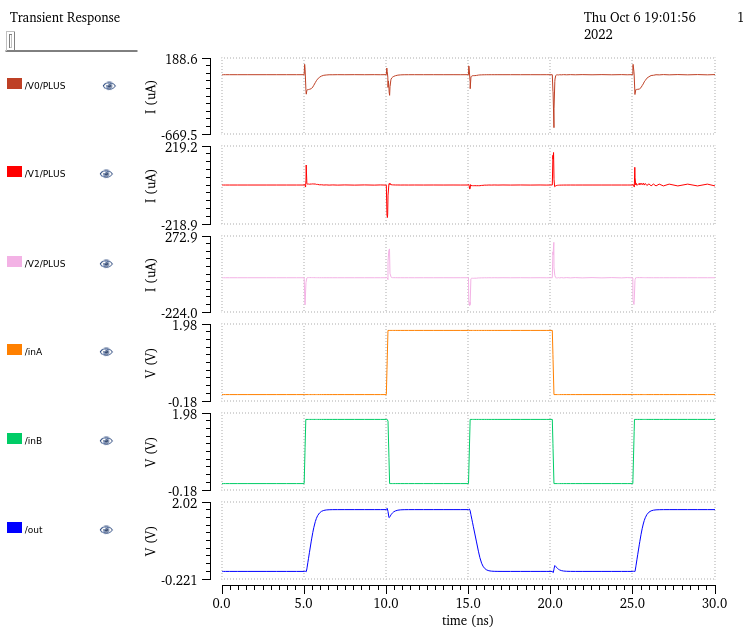
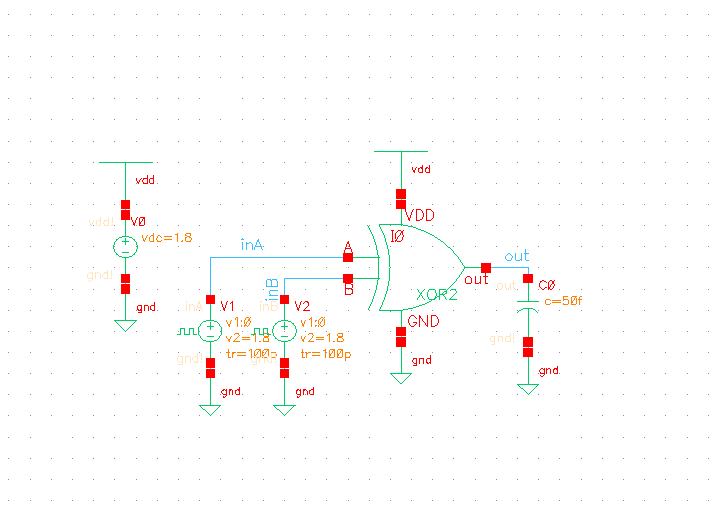


1. XOR2 Changes (Layout, LVS; no change to schematic)

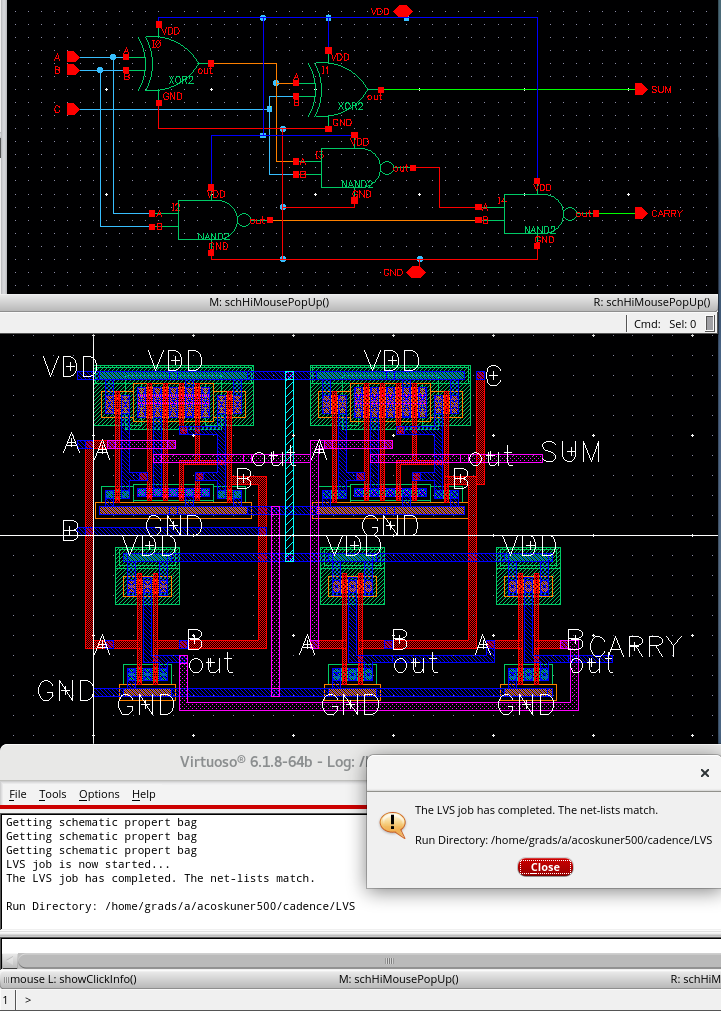


1. XOR2 Simulation

| XOR2 power VDD | -17.05E-6 |
| --- | --- |
| XOR2 inA vpulse average power | 128.4E-9 |
| XOR2 inB vpulse average power | -472.8E-9 |
| XOR2 rising delay | 3.85E-10 |
| XOR2 falling delay | 4.19E-10 |

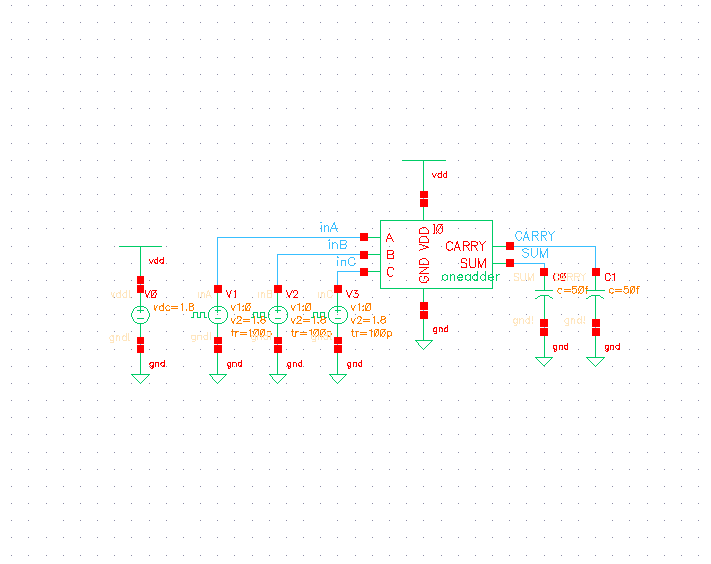


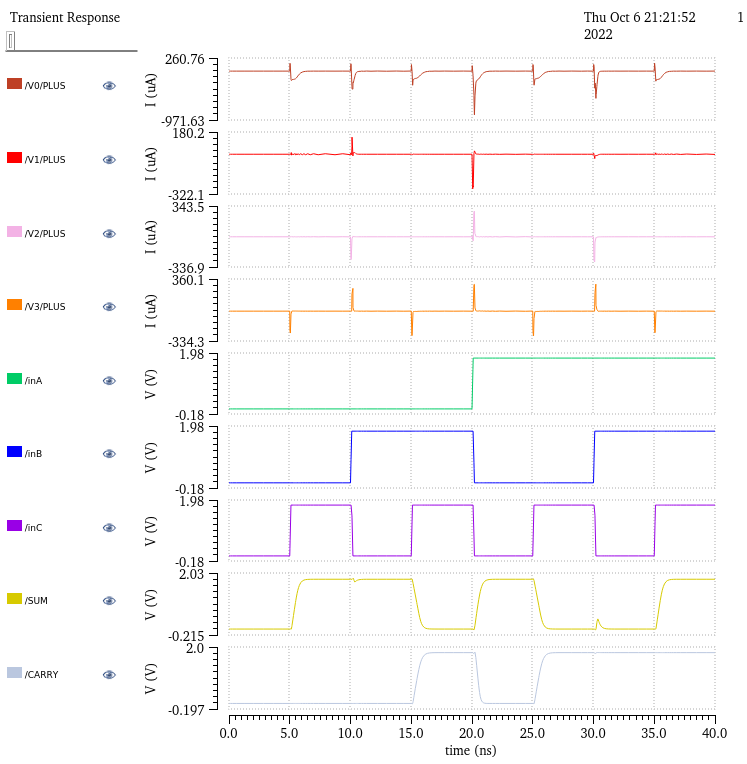
1. 1-bit adder (schematic, layout, DRC, LVS)



1. 1-bit adder Simulation

| Full Adder VDD Average power | -33.89E-6 |
| --- | --- |
| Full Adder inA vpulse average power | -461.7E-9 |
| Full Adder inB vpulse average power | -596.4E-9 |
| Full Adder inC vpulse average power | -419.2E-9 |
| Full Adder SUM rising delay | 4.00E-10 |
| Full Adder SUM falling delay | 4.28E-10 |
| Full Adder CARRY rising delay | 4.37E-10 |
| Full Adder CARRY falling delay | 3.37E-10 |





1. 1-bit Adder Max Frequency: 1/3ns = 333MHz

